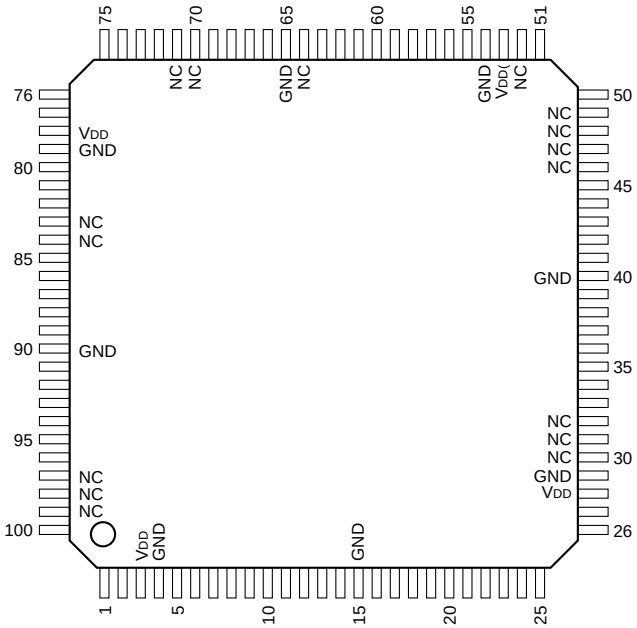
## C-MOS SDDI INTERFACE (GATE ARRAY)

—TOP VIEW—




| PIN NO. | I/O | SIGNAL | PIN NO. | I/O | SIGNAL | PIN NO. | I/O | SIGNAL | PIN NO. | I/O | SIGNAL |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 1 | I | REFF | 26 | O | SYSH | 51 | O | $\overline{\text{SWDET}}$ | 76 | O | TP0 |
| 2 | I | $\overline{\text{RST}}$ | 27 | O | SYSV | 52 | — | NC | 77 | I | TEST |
| 3 | — | VDD | 28 | — | VDD | 53 | — | VDD | 78 | — | VDD |
| 4 | — | GND | 29 | — | GND | 54 | — | GND | 79 | — | GND |
| 5 | I/O | SYSIO0 | 30 | — | NC | 55 | I | APDEP0 | 80 | I | CK |
| 6 | I/O | SYSIO1 | 31 | — | NC | 56 | O | ADEN0 | 81 | I | SOPMD |
| 7 | I/O | SYSIO2 | 32 | — | NC | 57 | O | AINT0 | 82 | I | CIFMD |
| 8 | I/O | SYSIO3 | 33 | I | $\overline{\text{OENBL}}$ | 58 | I | APDEP1 | 83 | — | NC |
| 9 | I/O | SYSIO4 | 34 | O | PRTYO | 59 | O | ADEN1 | 84 | — | NC |
| 10 | I/O | SYSIO5 | 35 | O | DOUT0 | 60 | O | AINT1 | 85 | I | DIN0 |
| 11 | I/O | SYSIO6 | 36 | O | DOUT1 | 61 | I | APDEP2 | 86 | I | DIN1 |
| 12 | I/O | SYSIO7 | 37 | O | DOUT2 | 62 | O | ADEN2 | 87 | I | DIN2 |
| 13 | I | STAT1 | 38 | O | DOUT3 | 63 | O | AINT2 | 88 | I | DIN3 |
| 14 | I | $\overline{\text{CCS}}$ | 39 | O | DOUT4 | 64 | — | NC | 89 | I | DIN4 |
| 15 | — | GND | 40 | — | GND | 65 | — | GND | 90 | — | GND |
| 16 | I | STAT0 | 41 | O | DOUT5 | 66 | O | SUOP1 | 91 | I | DIN5 |
| 17 | I | $\overline{\text{STRB}}$ | 42 | O | DOUT6 | 67 | O | SUOP0 | 92 | I | DIN6 |
| 18 | I | CADRS1 | 43 | O | DOUT7 | 68 | I | SUIP1 | 93 | I | DIN7 |
| 19 | I | CADRS2 | 44 | O | DOUT8 | 69 | I | SUIP0 | 94 | I | DIN8 |
| 20 | I | CADRS3 | 45 | O | DOUT9 | 70 | — | NC | 95 | I | DIN9 |
| 21 | I | CADRS4 | 46 | — | NC | 71 | — | NC | 96 | I | PRTYI |
| 22 | I | CADRS5 | 47 | — | NC | 72 | O | TP4 | 97 | — | NC |
| 23 | I | CADRS6 | 48 | — | NC | 73 | O | TP3 | 98 | — | NC |
| 24 | I | CADRS7 | 49 | — | NC | 74 | O | TP2 | 99 | — | NC |
| 25 | O | SYSF | 50 | O | $\overline{\text{PCERD}}$ | 75 | O | TP1 | 100 | I | REFH |

**INPUT**

| | |
|---|---|
| APDEP0 - APDEP2 | ; CH-0, 1, 2 DATA END |
| CADRS1 - CADRS7 | ; ADDRESS |
| $\overline{CCS}$ | ; CHIP SELECT |
| CIFMD | ; CPU I/F MODE SETTING |
| CK | ; SYSTEM CLOCK |
| DIN0 - DIN9 | ; PARALLEL DATA |
| $\overline{OENBL}$ | ; DIN0 - DIN9 OUTPUT ENABLE |
| PRTYI | ; DIN0 - DIN9 PARITY |
| REFF | ; REFERENCE FRAME |
| REFH | ; REFERENCE H |
| $\overline{RST}$ | ; SYSTEM RESET |
| SOPMD | ; $\overline{TX}$/RX MODE SETTING |
| STAT0, STAT1 | ; BUS STATUS 0, 1 |
| $\overline{STRB}$ | ; STROBE |
| SUIP0, SUIP1 | ; INPUT PORT 0, 1 |
| TEST | ; TEST FOR IC (GND CONNECT) |

**OUTPUT**

| | |
|---|---|
| ADEN0 - ADEN2 | ; CH-0, 1, 2 DATA ENABLE |
| AINT0 - AINT2 | ; CH-0, 1, 2 INTERRUPT |
| DOUT0 - DOUT9 | ; PARALLEL DATA |
| $\overline{PCERD}$ | ; PAYLOAD CRCC ERROR DETECT |
| PRTYO | ; DOUT0 - DOUT9 PARITY |
| SUOP0, SUOP1 | ; OUTPUT PORT 0, 1 |
| $\overline{SWDET}$ | ; SWITCHING DETECT |
| SYSF | ; REFERENCE FRAME |
| SYSH | ; REFERENCE H |
| SYSV | ; V BLANKING |
| TP0 - TP4 | ; TEST POINT 0 - 4 |

**INPUT/OUTPUT**

| | |
|---|---|
| SYSIO0 - SYSIO7 | ; DATA BUS |